LBNE Water Cherenkov Electronics Reference Design

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1 Introduction

This document describes a hypothetical design for readout of a large water Cherenkov detector, with about 50,000 photomultiplier tubes. It is intended to serve as the basis of a detailed cost estimate and schedule for the LBNE experiment. It should not be interpreted as a preliminary design the actual instrumentation selected for the experiment may be quite different

2 Assumptions

- The following assumptions are made to constrain the parameter space for the design:
- Each PMT is equipped with a passive voltage divider, and is operated with its photocathode at ground potential (positive high voltage configuration)
- Each PMT has one coaxial cable routed from the PMT to an electronics rack located above water. This cable carries the PMT bias voltage and anode signal. The cables are assumed to be *equal length* at least within large regions of the detector.
- All electronics is mounted in standard 19 inch rack-mount cabinets
- Provisions are made to read out every PMT pulse via Ethernet to a computer farm using standard network hardware. This is the basis for a software trigger as well as DAQ.
- Provisions are also made for a hardware trigger (current sum proportional to number of PMT hits within coincidence window)

3 Modularity

The following modularity is assumed. This is quite arbitrary, but some choice must be made. The cost estimate will parameterize this to allow for comparison between various configurations.

- 16 PMTs supplied by one high voltage generator (or one channel of a multi-channel supply) on a single circuit card

- Individual HV disable and voltage trim per PMT (may be manual)
- 16 HV circuit cards mounted in a 19 inch enclosure ("crate")
- Two enclosures mounted in a rack (512 PMTs per rack)

It is anticipated that the readout electronics will fit within this same envelope, either by combining HV with readout in the same crate, or by making the crates sufficiently compact that a total of four smaller crates fit within a rack.

4 Implementation

4.1 PMT Bases and Cables

This document does not cover the detailed design of the PMT bases and cables, but certain criteria must be met in the design of these items to ensure good performance of the readout system. The bases must include accurate back-termination circuitry to cancel any reflections which may result from impedance mis-match at the readout end.

Should we state any assumptions about the cables here??

4.2 Racks

The electronics will be installed in standard 19 inch racks. The racks will contain at least the following:

- **Power Management** – Provides current limiting and power distribution for AC power within the rack. Emergency shutdown and fire protection interlocks may be included as required by laboratory policy.
- **Network Switch** – Commercial rack-mount network switch which provides access to Ethernet on the electronics.
- **Power Supplies** – Bulk DC power supplies for the electronics. At least control and monitoring should be provided on the front panel. The supplies themselves may be mounted in the rear of the rack.
- **Electronics Crates** – These enclosures will house vertically-mounted electronics boards. There may be two or four crates per rack depending on implementation details.
- **Fan Trays** – Cooling for crates will be provided by vertical forced-air cooling. Each crate will have a fan tray below it to provide air flow.

The requirements document states that the electronics temperature must be kept within $\pm 1^{\circ}$C. This is a rather stringent requirement, which implies either a regulated, closed-loop cooling system in the racks, or that the racks themselves are enclosed in a trailer or hut with dedicated air conditioning.

4.3 Crates

One electronics crate services 256 electronics channels. Crates are 9U high and comply more or less with Eurocard mechanics (as used in VME systems). Slot spacing is one inch (as opposed to the 0.8 inch spacing in VME systems) to allow for better cooling and HV component clearance.

The coaxial cables from 16 PMTs terminate on a connector panel at the rear of the crate. A pair of boards (readout, high voltage) provide power and signal processing. The two boards may both be removed from the front of the crate.

A side view of one crate slot is shown in Figure 1.

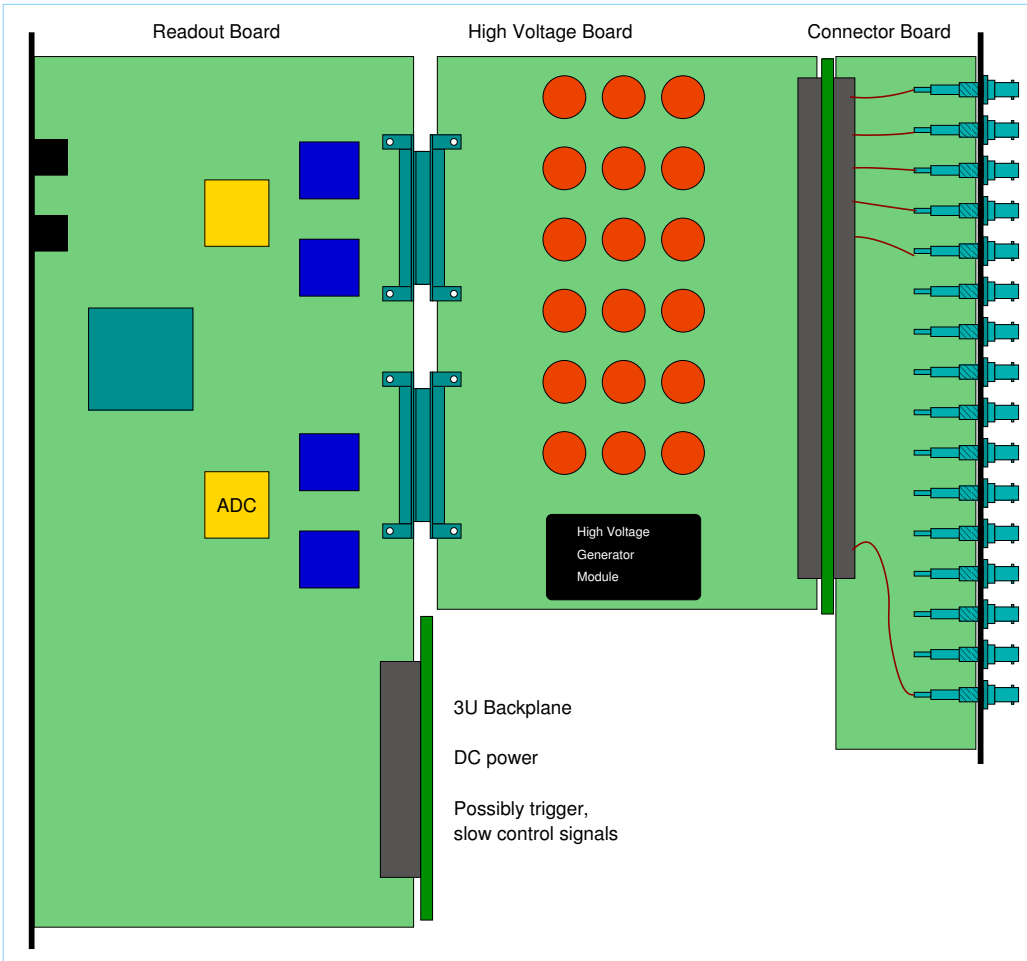

Figure 1: HV and Signal Board Arrangement

4.4 Connector Panels

A connector panel is mounted at the rear of the crate for each slot. For purposes of this document we assume that the cable is similar to RG-59/U coaxial cable, and that each cable has an SHV connector installed. This panel contains 16 SHV chassis connectors mounted on an aluminum panel, with a simple PC board or aluminum plate attached. On the plate or PCB is a right-angle board-to-board connector which carries the signals to the high voltage board. The connector panel has geometry similar to a VME rear transition module, though it is designed to be permanently installed and replaced only in case of connector failure.

4.5 High Voltage Boards

The high-voltage board is installed from the front of the crate and mates with the connector panel. The high-voltage board decouples signals from the cables and routes them through the backplane to a readout board. The RTM also provides high voltage using an on-board high voltage generator (DC-DC converter module).

DC power for the high voltage generator is provided from the backplane. Individual high voltage trim circuits, with voltage and current readback are provided. Control and monitoring circuits will be controlled from the readout board by I^2C or similar low-speed serial bus.

The high-voltage board will contain a programmable test pulse generator circuit which may be enabled on a per-channel basis. This pulse generator will have a programmable amplitude range suitable for (relative) calibration and test of the entire readout chain.

4.6 Per-Channel Signal Processing

For each PMT signal, HV is decoupled from the signal, and pulse arrival time and integrated charge are digitized. Please refer to Figure 3 for a block diagram of a single channel.

The signal is decoupled from the DC high voltage bias by a blocking capacitor. Following the capacitor is discharge protection circuitry which will prevent damage to the readout electronics in the event a sudden discharge of the blocking capacitor occurs. The high voltage bias supply for the PMT is coupled to the cable through a current-limiting resistor.

The **preamp** terminates the cable at the correct impedance, provides gain as required, and may include equalization circuitry to compensate for cable dispersion and attenuation.

The preamp has two analog outputs: one to drive the input of the shaper, and another to drive the discriminator input. A third monitor output may be provided for diagnostic purposes (perhaps for one channel only to save pins).

The **shaper** provides baseline restoration and charge integration functions. A sample/hold function or gated integrator may be provided in this block, depending on the detailed design chosen. The output of the shaper is a relatively slow buffered analog signal which may be sampled using an external ADC. The shaper may provide one or more monitoring outputs for diagnostic purposes.

The **analog delay** delays the shaped analog signal so that it may be sampled in response to the discriminator output. The analog delay output may driven on an output pin in real-time, or

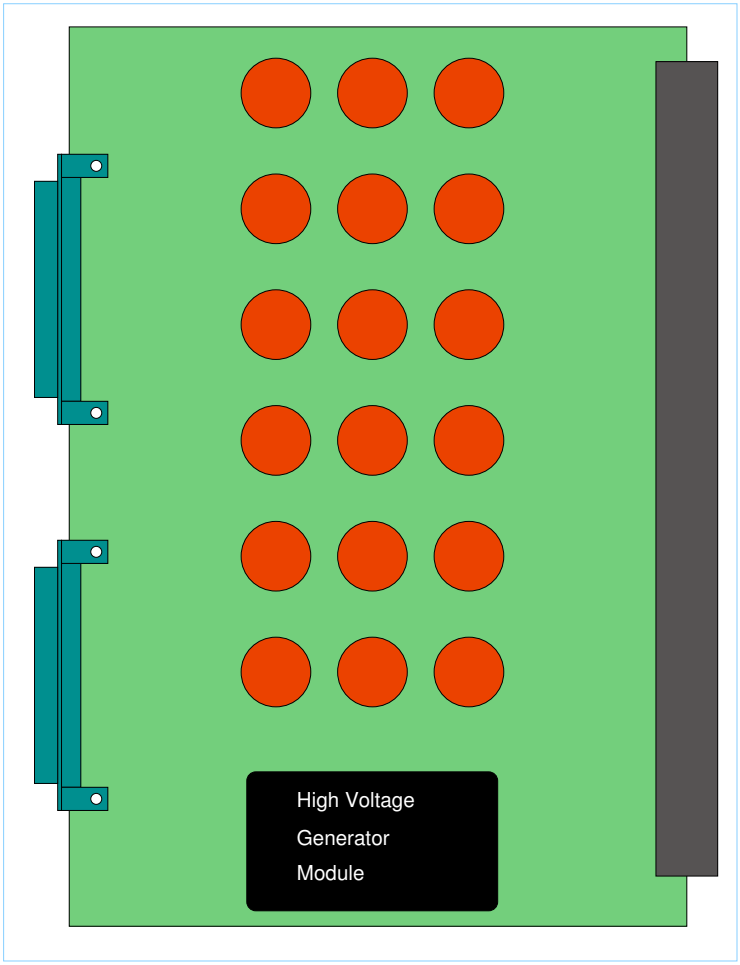

Figure 2: High Voltage Board

an analog memory to store integrated charge for later digitization may be provided.

The **discriminator** performs two functions. First, it provides a low-threshold trigger to activate the digitizing and recording logic for a channel. Second, it measures the mean arrival time of a light pulse using a constant-fraction or peak-finding function. The discriminator also provides an analog sum of the discriminator outputs for use in a hardware trigger. Logic triggered by the discriminator output will initiate digitization of the shaper output by an ADC.

These functions will be performed by 4 multi-channel application-specific integrated circuits (ASICs). The first ASIC (the "Analog ASIC") provides the pre-amplifier, shaper and analog delay functions. The second ASIC provides the discriminator functions.

Time measurement is provided by a TDC implemented in an FPGA. Multi-channel TDC implementations based on tapped delay lines exist today with time resolution near 50ps, more than

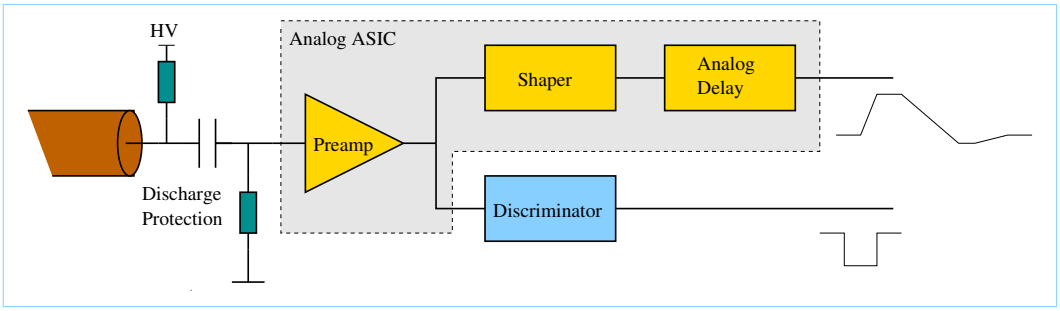

Figure 3: Single Channel Signal Processing

good enough to meet LBNE requirements.

4.7 16 Channel Readout Board

16 channels of PMT signals are processed as described above on a single PCB. Each analog ASIC and each discriminator ASIC processes 4 channels, so four of each are mounted on a 16 channel readout board, as shown in Figure 4. A logical block diagram of the readout board is shown in Figure 5.

The shaped analog signals are digitized by a multiplexed ADC with integrated sample/hold circuitry. This may be either a commercial device, a third type of ASIC, or a combination of the two. Control is provided by an FPGA with attached SDRAM buffer memory.

All control and readout for each 16 channel board is provided by a single Ethernet interface. The Ethernet physical interface (PHY) is provided by a commercial IC, while the MAC and higher-level protocol functions will be provided within the FPGA.

Each readout card will be equipped with sufficient memory for 10^6 events on-board storage (about 128 MBytes) to handle a nearby supernova or other burst.

4.8 Clock and Controls

A global clock and timing distribution system is required. A 10 MHz reference clock and 1 pps time marker are distributed as differential signals on a Cat-6 class network cable. The time marker may be augmented by a coded time-of-day signal to ensure synchronization between all elements of the data acquisition system.

A "tree" fanout system for the clock/controls system is the simplest architecture. A 32-port fanout module services each rack, with 4 to 8 additional fanout modules required to distribute signals from a single master point.

"Slow" controls (initialization and monitoring of the DAQ hardware) would be entirely handled over the same Ethernet path as that used for data acquisition. Thus no additional "crate controller" modules are required.

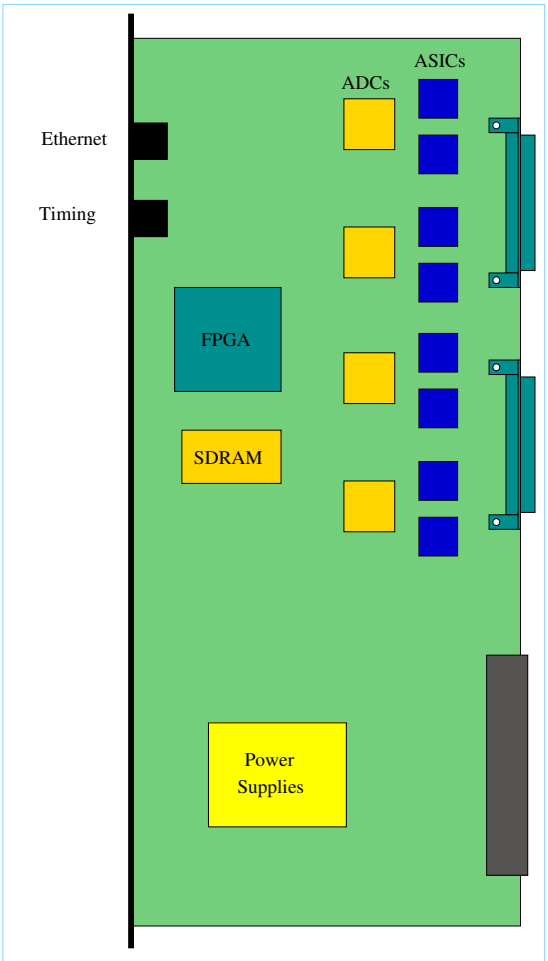

Figure 4: 16-Channel Readout Board

4.9 Hardware Trigger

A hardware trigger is an optional feature of the reference design. It would be used as a diagnostic tool to easily monitor detector behavior independent of the software trigger and also as a potential back for the software trigger.

Each readout module provides an analog sum of 16 discriminator outputs as a current signal on one pair of an RJ-45 connector. To implement a hardware trigger, this signals would be added using a combination of analog and digital circuitry to provide a global “n tubes” coincidence within a programmable window.

Implementation of the hardware trigger would require one trigger sum module per crate, plus regional sum modules feeding a global trigger processor of some sort.

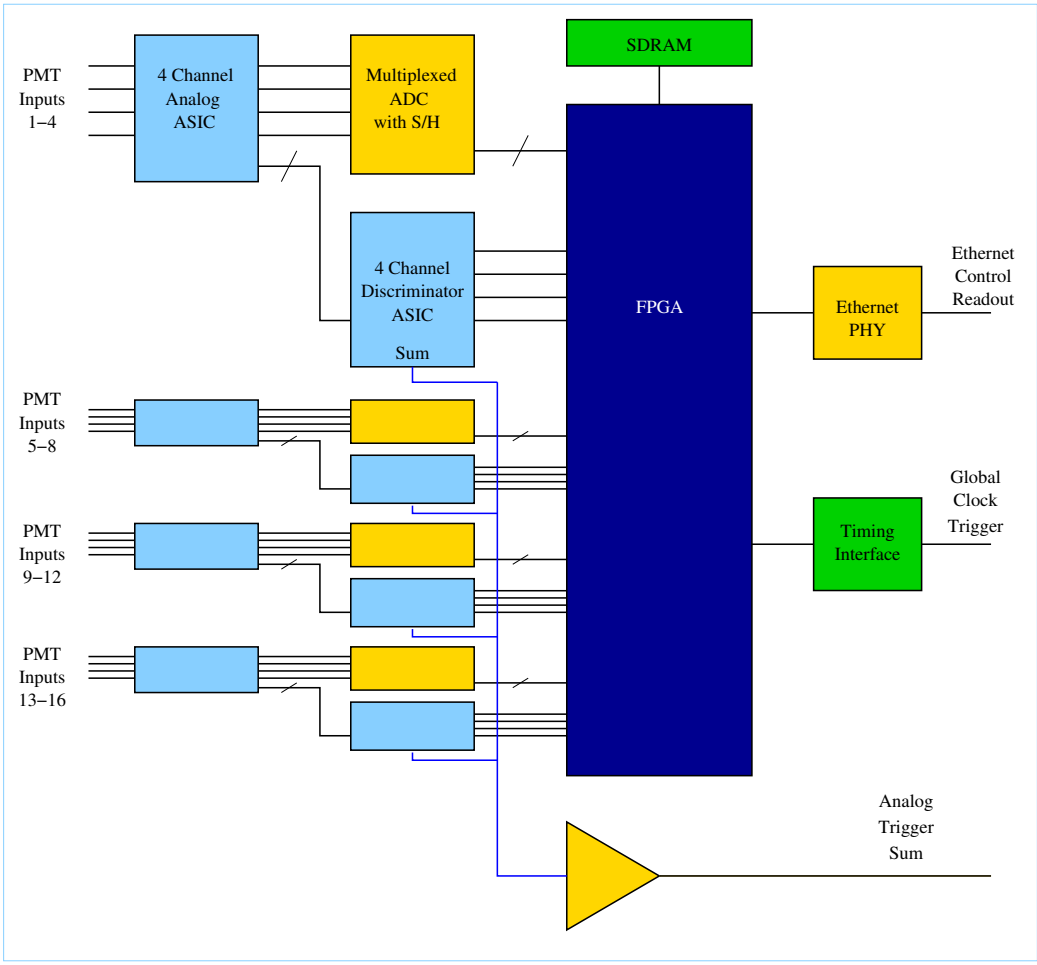

Figure 5: 16-Channel Readout Board Block Diagram

4.10 Software Trigger and Data Acquisition

The primary trigger and data acquisition is implemented in software. Each readout module provides one 100BaseT or 1GbE (1 gigabit) Ethernet output. It is anticipated that the entire software trigger and data acquisition system will be built using off-the-shelf network and computing hardware. The following description is a tentative one based on technology available at the time this document is created. Table 1 lists the assumptions for data rate and volume.

It is assumed that there is sufficient memory on the front-end board to handle bursts from i.e. supernovae. The rate of neutrino and cosmic ray events is negligible compared to PMT dark noise, so we may safely use the dark noise rate for average bandwidth requirements.

Each front-end board contains a GbE interface, large SDRAM buffer, and sufficient FPGA resources to support one open TCP protocol connection per DAQ computer (48 connections in this

Parameter	Value	Notes
Total PMT count	50,000	
PMTs per rack	512	
PMT Dark Noise Rate	10 kHz	
Bytes per hit	8 bytes	32 bits time, 16 bits channel no., 16 bits charge

Table 1:

reference design). For one board (16 PMTs), we expect an average data rate due to PMT dark noise of $16 * 10^4 * 8 = 1.3$MBytes/s.

One example of how a data acquisition and software trigger system might be assembled is shown in Figure 6. Output data from 16 readout boards (one crate) is merged in one 16-port Ethernet switch. There are 192 switch outputs carrying about 20 MB/s each.

These 192 switch outputs are connected to 192 ports on 48 computers (each with a 4 port network interface card) through two layers of GbE switches to provide a switch fabric similar to a crosspoint. Each DAQ computer will open a TCP connection to each front-end board (3072 simultaneous connections per computer). The PMT hits will be multiplexed to the DAQ computers in a simple way, i.e. by time multiplexing where each computer receives all PMT hits for a 100ms time period in round-robin fashion. The multiplexing will be accomplished by sorting the hits by timestamp on the readout board and assigning them to the appropriate TCP connection queue.

The first-level software trigger is a simple algorithm whereby a trigger is generated whenver more then N hits are seen in a sliding coincidence window. It is anticipated that the rate of saved data is of rough order 100 Hz with roughly 100 PMTs hit. This corresponds to a saved data rate of about 80 kB/s which is very comfortably accommodated by one Ethernet switch output.

5 Hardware Inventory

Table 2 summarizes the major hardware components required to build the reference system as described in this document.

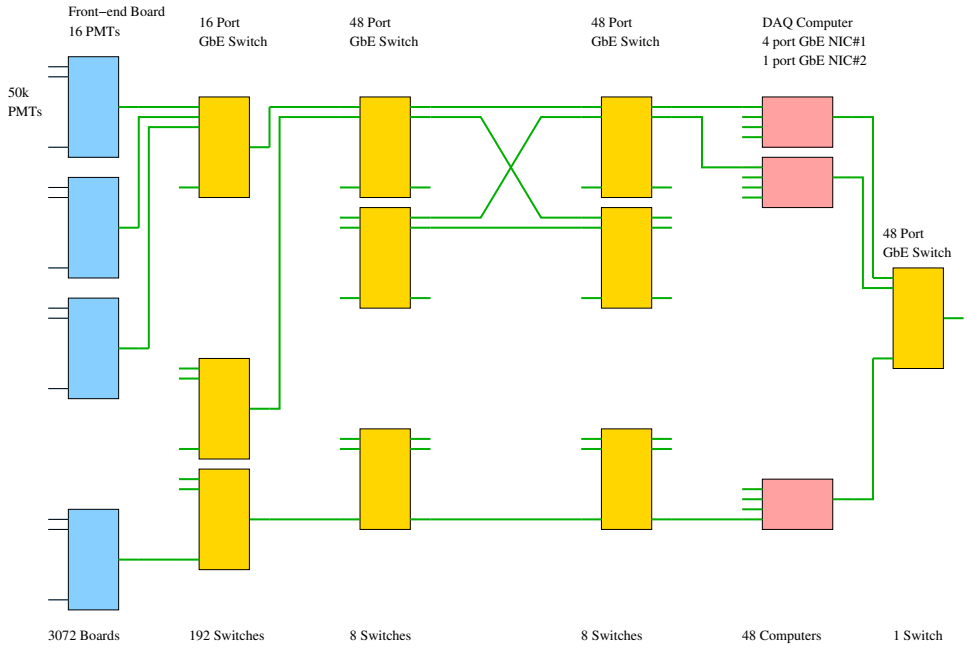

Figure 6: Software Trigger and Data Acquisition Hardware

Quantity	**Description**	**Notes**
50,000	PMT bases and cables	
3,125	High Voltage boards	
3,125	Readout boards	
12,500	Analog ASICs	
12,500	Discriminator ASICs	
196	16+1 port Gigabit Ethernet switches	
16	48 port Gigabit Ethernet switches	
48	DAQ computers	
200	custom crates with backplanes	
100	racks with cooling	
100	bulk DC power supplies	
100	32-channel custom timing fanout modules	
8	master timing fanout modules	

Table 2: Reference System Major Hardware Components